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(54) **SEMICONDUCTOR MEMORY DEVICES AND MEMORY SYSTEMS INCLUDING THE SAME**

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(57) **ABSTRACT**

A semiconductor memory device is provided. The semiconductor memory device includes a memory cell array, an input/output (I/O) gating circuit and an error correction circuit. The memory cell array includes a plurality of memory cells. The I/O gating circuit, before performing a normal memory operation on the memory cell array by a first unit, performs a cell data initializing operation by writing initializing bits in the memory cell array by a second unit different from the first unit. The error correction circuit performs an error correction code (ECC) encoding and an ECC decoding on a target page of the memory cell array by the second unit, based on the initializing bits. Therefore, power consumption in performing write operation may be reduced.